

# A DETERMINISTIC SCHEDULING APPROACH FOR WAFER FABRICATION FACILITIES

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**Abstract:** The primary goal of our proposed research effort is to develop solution methodologies for minimizing total weighted tardiness (TWT) for wafer fabrication facilities. We have taken the first steps towards this goal. In Mason et al. [1], we extended the classical job shop work of Pinedo and Singer [2] and developed a disjunctive graph formulation of the problem. Unlike previous job shop scheduling efforts, our disjunctive graph formulation accounts for batching tools, tool groups (identical machines operating in parallel), sequence-dependent setup times, and recirculating product flow. We provide some computational results that show the effectiveness of our approach.

**Key words:** Heuristic, Semiconductor Manufacturing, Total Weighted Tardiness.

## 1. OVERVIEW

Manufacturing integrated circuits on raw silicon wafers, also called (semiconductor manufacturing, is one of the most complex manufacturing processes in existence today. Semiconductor manufacturing consists of four major steps: 1) wafer fabrication, 2) sort or probe, 3) assembly/packaging, and 4) final test. Wafer fabrication is the most expensive and time consuming of these steps. In wafer fabrication, individual wafers of a given product (job) type are required to complete 300–400 process steps as they move through the wafer fabrication facility (wafer fab) in groups or lots of various size (for example, 25 wafers). Each lot of wafers competes with hundreds of other lots for processing time on the wafer fab's 50–100 different tool groups. The economic necessity to reduce capital spending dictates that such expensive machines be shared by all lots requiring the particular processing operation provided by the machine, even though they may be at different stages of their manufacturing cycle. These tool groups, which have machines that can range in price from \$100,000 to \$14,000,000, typically contain a number of identical machines operating in parallel, some of which may be dedicated to the production of one or more products. This results in a manufacturing environment that is different in several ways from both traditional flow shops as well as job shops (see Figure 1). The main consequence of the re-entrant flow nature is that wafers at different stages in their manufacturing cycle have to compete with each other for the same machines. The manner in which this competition is resolved has a clear impact on plant performance measures, particularly those related to meeting customer due dates.

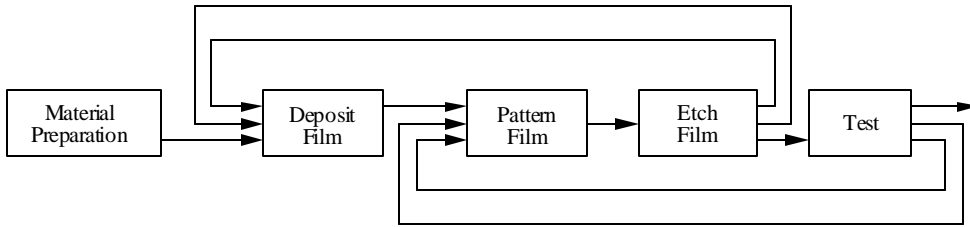


Figure 1. The wafer fabrication process (Re-entrant Flow)

In most wafer fabs today, the competition is resolved using dispatching techniques. In this presentation, we discuss our research efforts to develop deterministic scheduling solution methodologies for minimizing total weighted tardiness (TWT) for wafer fabrication facilities. We have taken the first steps towards this goal. In Mason *et al.* [1], we extended the classical job shop work of Pinedo and Singer [2] and developed a disjunctive graph formulation of the  $FJc | r_j, s_{jk}, B, recrc | \sum w_j T_j$  problem. Unlike previous job shop scheduling efforts, our disjunctive graph formulation accounts for batching tools, tool groups (identical machines operating in parallel), sequence-dependent setup times, and recirculating product flow. We provide an overview of our basic approach, briefly discuss the process of embedding our deterministic scheduling approach into a discrete event simulation, and present a comparison of our results with dispatching approaches on a variety of data sets.

## REFERENCES

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